

MR1035-1477

Serial Number: 10/092,392

Reply to Office Action dated 3 November 2004

### AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in the Application.

#### Listing of Claims:

Claim 1 (Currently amended): A method of providing forward error correction (FEC) to a data frame on a plurality of frame packets, the method comprising the steps of:

packetizing the data frame into a plurality of frame packets;

selecting ~~concatenating~~ selected portions of packet data from each of the  
corresponding to a plurality of frame packets for a first frame;

generating a forward error correction code bits for the ~~concatenated~~  
selected portions of packet data exclusive of corresponding remaining portions of  
each of the plurality of frame packets; and

transmitting separately the forward error correction code bits and the  
plurality of frame packets, in a separate the packet containing the forward error  
correction code being identified with a user data identifier code.

Claim 2 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein the transmission of the forward error correction code bits in the separate packet is MPEG-4 compliant.

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Claim 3 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein further including the step of transmitting the plurality of frame packets temporally prior to the separate forward error correction code packet transmitting step is transmitted after the plurality of frame packets.

Claim 4 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein the forward error correction code generating step includes the step of generating the forward error correction code bits are generated using as a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 5 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein the forward error correction code generating step includes the step of generating the forward error correction code bits are generated using as a systematic code.

Claim 6 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein the packetizing step includes the step of separating the selected portions of packet data includes into at least portions respectively and separately containing motion vector data and Discrete Cosine Transform (DCT) data.

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Claim 7 (Currently amended): The method as ~~defined~~ recited in claim 6 ~~+~~, wherein the packet data selecting step includes the step of selecting as the selected portions of packet data includes only header data, the motion vector data and and one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 8 (Currently amended): The method as ~~defined~~ recited in claim 1, wherein the packet data selecting step includes the step of selecting as the selected portions of packet data corresponds to only packet data located between a resync field and a motion marker.

Claim 9 (Currently amended): The method as ~~defined~~ recited in claim 1, further comprising the steps of:

setting a flag indicating that a fixed Video Object Plane (VOP) increment is to be used set a fixed interval between each of the plurality of frame packets; and assigning providing a corresponding fixed time increment value to the fixed Video Object Plane increment.

Claim 10 (Currently amended): The method as ~~defined~~ recited in claim 1, further comprising the step of transmitting in the separate forward error correction code packet a value for at least a first of the plurality of frame packets related to

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indicating a quantity of bits within the at least a first packet of the plurality of frame packets for which the forward error correction code bits are generated.

Claim 11 (Currently amended): An error correction generating circuit, comprising:

a processor coupled to a processor readable memory;

a first instruction sequence stored in the processor memory and operable to cause the processor to select portions of packet data from each of a plurality of frame packets of a corresponding packetized data frame;

a first ~~second~~ instruction sequence stored in the processor readable memory configured and operable to cause the processor to generate forward error correction data for the selected portions of packet data exclusive of the remaining portions of each of the that are to be transmitted in a corresponding plurality of frame packets;

a ~~second~~ ~~third~~ instruction sequence stored in the processor readable memory configured and operable to cause the processor to store the forward error correction data in a first packet separate from the plurality of frame packets; and

a ~~third~~ ~~fourth~~ instruction sequence stored in the processor readable memory configured and operable to cause the processor to identify the first separate packet with a first data identifier code.

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Claim 12 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, further comprising a ~~fourth~~ fifth instruction sequence stored in the processor readable memory and operable to cause the processor configured to concatenate the selected portions of packet data before the first second instruction sequence is executed ~~generates the forward error correction data.~~

Claim 13 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, further comprising a ~~fourth~~ fifth instruction sequence stored in the processor readable memory and operable to cause the processor configured to set a flag indicating that a fixed Video Object Plane (VOP) increment is to be used set a fixed interval between each of the plurality of frame packets and to provide assign a corresponding fixed time increment value thereto.

Claim 14 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, further comprising a ~~fourth~~ fifth instruction sequence stored in the processor readable memory and operable to cause the processor configured to provide a Header Extension Code (HEC) in a every packet in a first sequence of packets.

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Claim 15 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the error correction generation circuit is incorporated on an integrated circuit.

Claim 16 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the ~~first~~ separate packet is MPEG-4 compliant.

Claim 17 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the forward error correction data is generated using a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 18 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the forward error correction data is generated using a systematic code.

Claim 19 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the ~~selected portions of packet data~~ is separated into at least portions respectively and separately containing ~~includes~~ motion vector data and Discrete Cosine Transform (DCT) data.

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Claim 20 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 19 ~~44~~, wherein the selected portions of packet data includes only header data, the motion vector data and one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 21 (Currently amended): The error correction generation circuit as ~~defined~~ recited in claim 11, wherein the selected portions of packet data ~~corresponds to~~ is only the packet data located between a resync field ~~filed~~ and a motion marker.

Claim 22 (Currently amended): An encoder circuit, comprising:

a means for generating forward error correction data for selected portions of packet data from each of a plurality of frame packets exclusive of the remaining portions of packet data in each of the plurality of frame packets;

a means for storing the forward error correction data in a ~~first~~ packet separate from the plurality of frame packets; and

a means for identifying the ~~first~~ separate packet with a ~~first~~ an identifier code.

Claim 23 (Currently amended): The encoder as ~~defined~~ recited in claim 22, further comprising a means for concatenating the selected portions of packet data.

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Claim 24 (Currently amended): The encoder as ~~defined~~ recited in claim 22, further comprising a means for transmitting in the ~~first~~ separate packet at least a ~~first value related to~~ indicating a quantity of bits within at least a first packet of the plurality of frame packets ~~the first packet~~ for which forward error correction bits ~~were~~ data was generated.